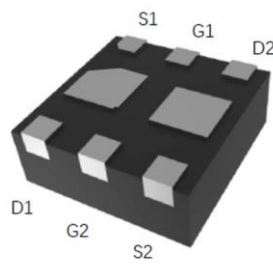
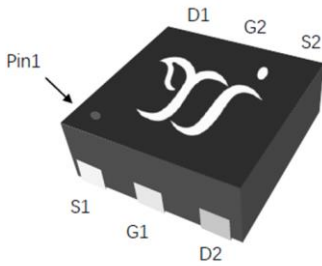


Dual N-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} 20V
- I_D 0.92A
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) $< 300m\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=2.5V$) $< 400m\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=1.8V$) $< 950m\Omega$
- ESD Protected Up to 2KV (HBM)

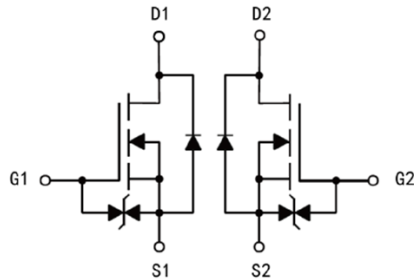
General Description

- High density cell design for Low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Interfacing, Logic switch
- Load switch
- Power management

DFN1010B-6L



Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V_{DS}	-	20	V
Gate-source Voltage			V_{GS}	-10	10	
Continuous Drain Current (Note 1,2)	Steady-State	$T_A=25^\circ C, V_{GS}=4.5V$	I_D	-	0.92	A
		$T_A=100^\circ C, V_{GS}=4.5V$		-	0.58	
Continuous Drain Current (Note 1,3)	Steady-State	$T_{SP}=25^\circ C, V_{GS}=4.5V$, Chip limitation		-	2.4	
		$T_{SP}=100^\circ C, V_{GS}=4.5V$		-	1.5	
Pulsed Drain Current	$T_A=25^\circ C, t_p \leq 10\mu s$		I_{DM}	-	3.68	
Maximum Body-Diode Continuous Current	$T_A=25^\circ C$		I_S		0.35	
Total Power Dissipation (Note 1,2)	Steady-State	$T_A=25^\circ C$	P_D	-	0.41	W
		$T_A=100^\circ C$		-	0.16	
Total Power Dissipation (Note 1,3)	Steady-State	$T_{SP}=25^\circ C$		-	2.77	
		$T_{SP}=100^\circ C$		-	1.11	
Junction and Storage Temperature Range			T_J, T_{STG}	-55	150	$^\circ C$

Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	300	$^\circ C/W$
Thermal Resistance Junction-to-Soldering Point	Steady-State	$R_{\theta JSP}$	-	45	



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■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A, T_j=25^\circ C$	20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V, T_j=25^\circ C$	-	-	1	μA
		$V_{DS}=2V, V_{GS}=0V, T_j=150^\circ C$	-	-	100	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 10V, V_{DS}=0V, T_j=25^\circ C$	-	-	± 10	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A, T_j=25^\circ C$	0.35	0.75	1.1	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=0.5A, T_j=25^\circ C$	-	170	300	$m\Omega$
		$V_{GS}=2.5V, I_D=0.4A, T_j=25^\circ C$	-	245	400	$m\Omega$
		$V_{GS}=1.8V, I_D=0.2A, T_j=25^\circ C$	-	400	950	$m\Omega$
Diode Forward Voltage	V_{SD}	$I_S=0.2A, V_{GS}=0V, T_j=25^\circ C$	-	0.74	1.2	V
Gate Resistance	R_G	$f=1MHz, T_j=25^\circ C$	-	8	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V, f=1MHz, T_j=25^\circ C$	-	29.3	-	pF
Output Capacitance	C_{oss}		-	11.4	-	
Reverse Transfer Capacitance	C_{riss}		-	4.7	-	
Switching Parameters						
Total Gate Charge	Q_g	$V_{GS}=4.5V, V_{DS}=10V, I_D=0.5A, T_j=25^\circ C$	-	0.47	-	nC
Gate-Source Charge	Q_{gs}		-	0.08	-	
Gate-Drain Charge	Q_{gd}		-	0.075	-	
Reverse Recovery Charge	Q_{rr}	$I_F=0.5A, di/dt=100A/\mu s, V_{GS}=0V, V_R=10V, T_j=25^\circ C$	-	2	-	nC
Reverse Recovery Time	t_{rr}		-	7.7	-	ns
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=4.5V, V_{DS}=10V, I_D=0.5A, R_{GEN}=10\Omega, T_j=25^\circ C$	-	3	-	ns
Turn-on Rise Time	t_r		-	4.4	-	
Turn-off Delay Time	$t_{D(off)}$		-	11.1	-	
Turn-off Fall Time	t_f		-	4.2	-	

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with $T_A=25^\circ C$. The maximum allowed junction temperature of 150 $^\circ C$. The value in any given application depends on the user's specific board design.
- Thermal resistance from junction to soldering point (on the exposed drain pad).



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Typical Electrical and Thermal Characteristics Diagrams

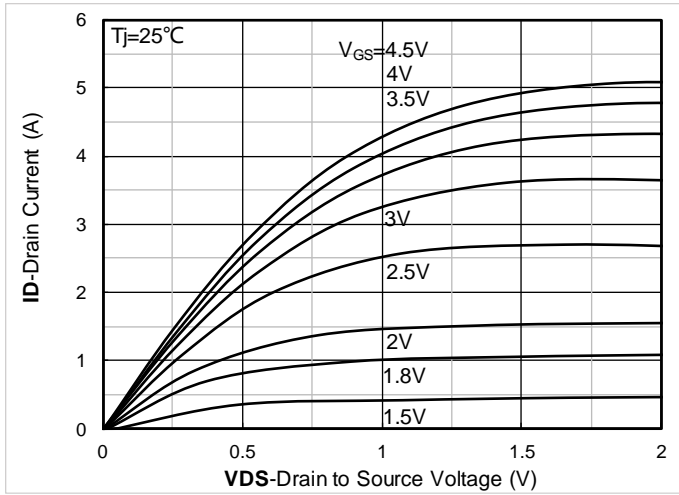


Figure 1. Output Characteristics; typical values

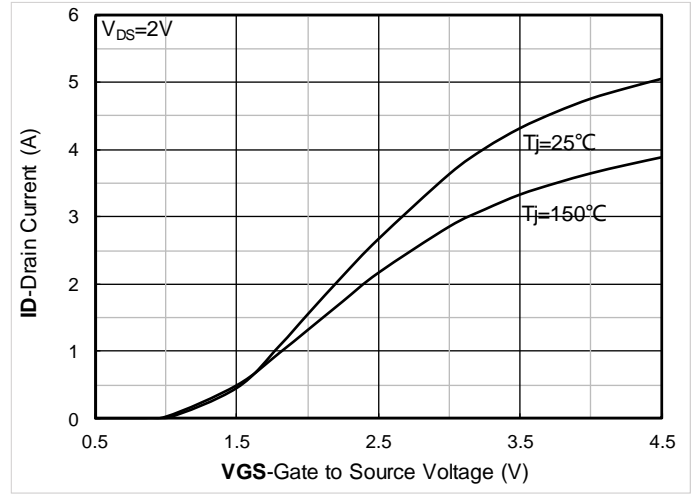


Figure 2. Transfer Characteristics; typical values

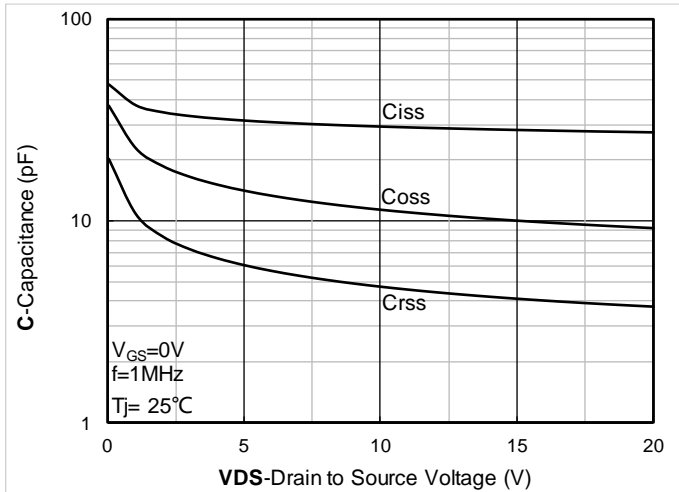


Figure 3. Capacitance Characteristics; typical values

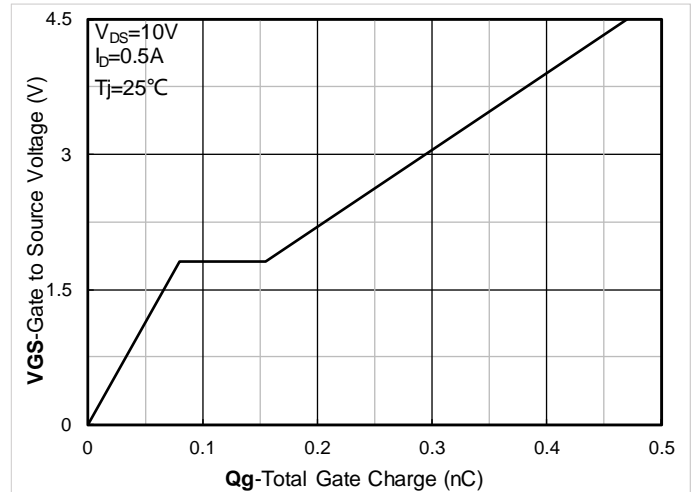


Figure 4. Gate Charge; typical values

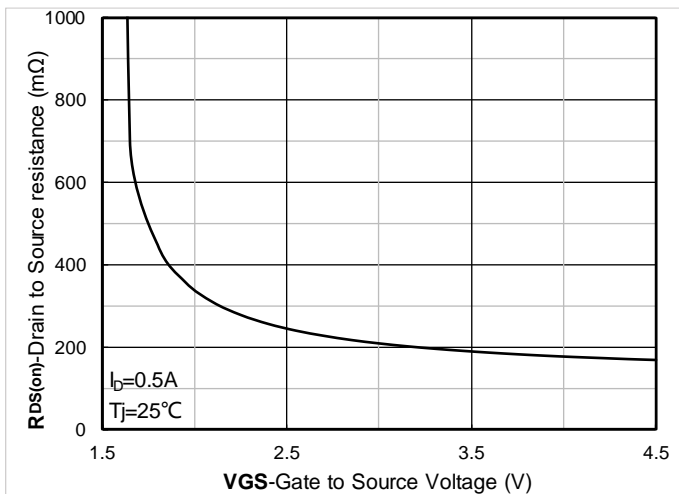


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

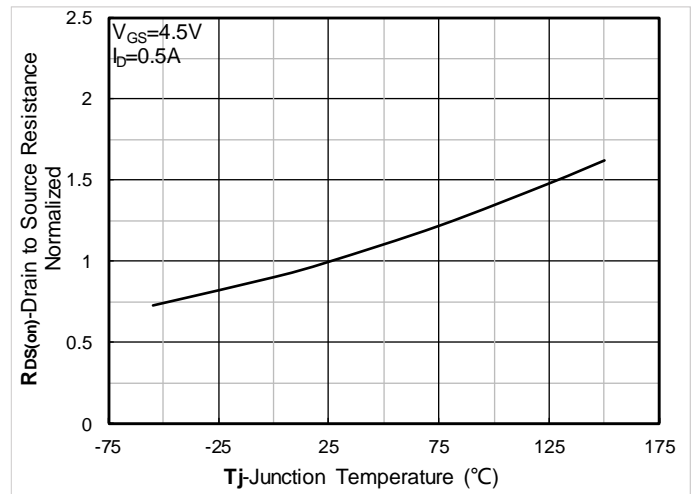


Figure 6. Normalized On-Resistance



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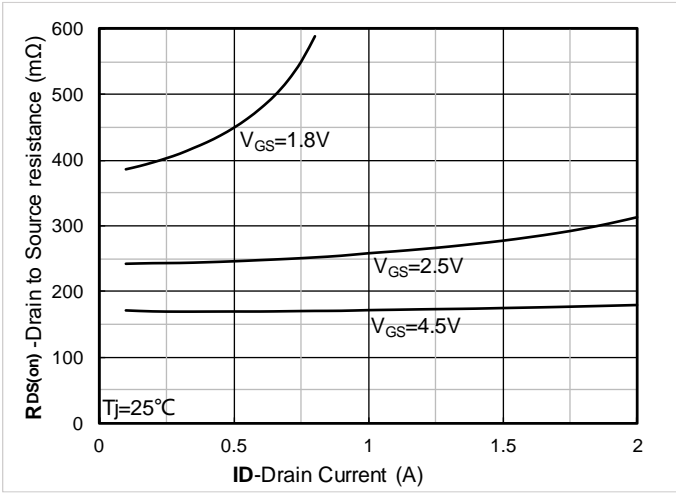


Figure 7. RDS(on) vs. Drain Current; typical values

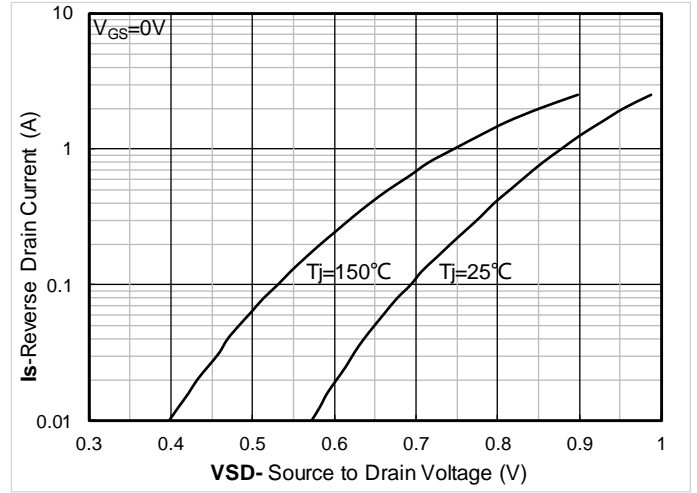


Figure 8. Forward characteristics of reverse diode; typical values

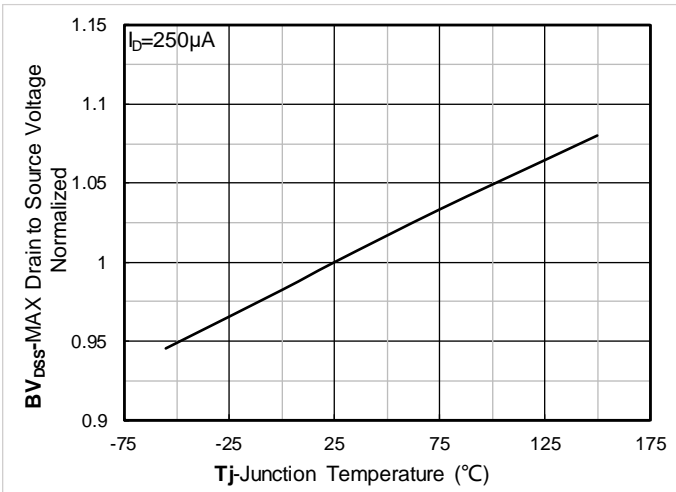


Figure 9. Normalized breakdown voltage

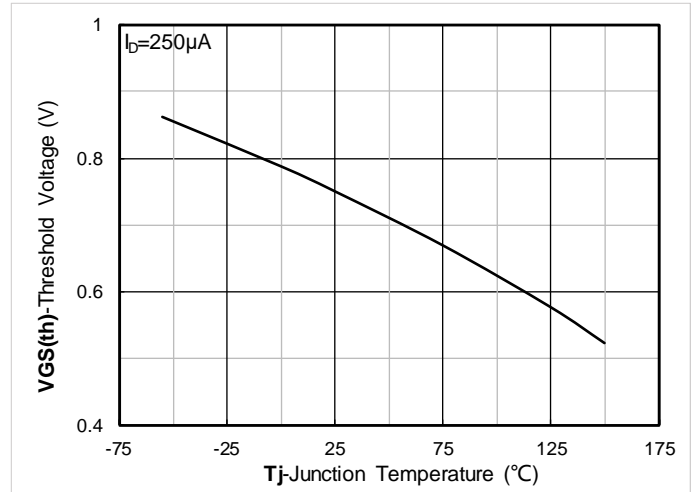


Figure 10. Gate Threshold voltage; typical values

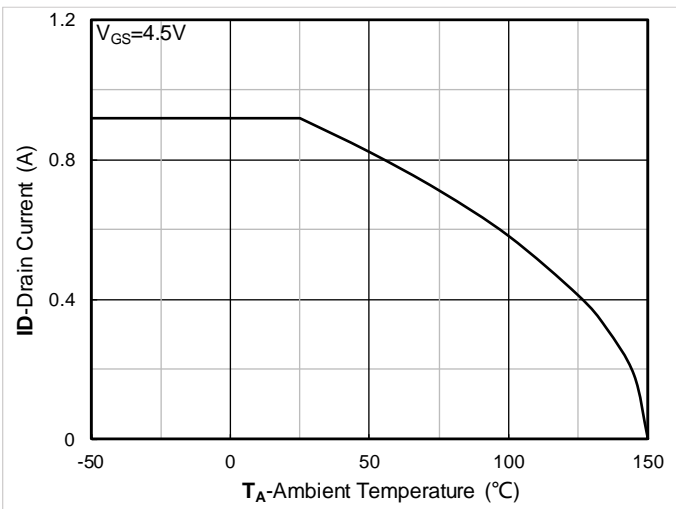


Figure 11. Current dissipation

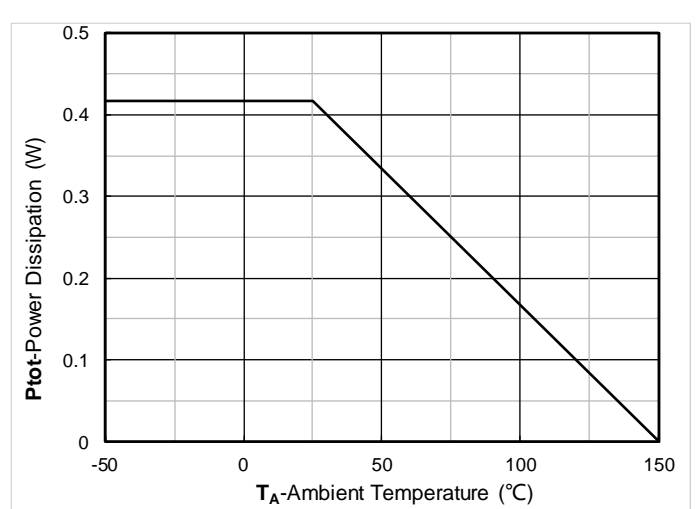


Figure 12. Power dissipation



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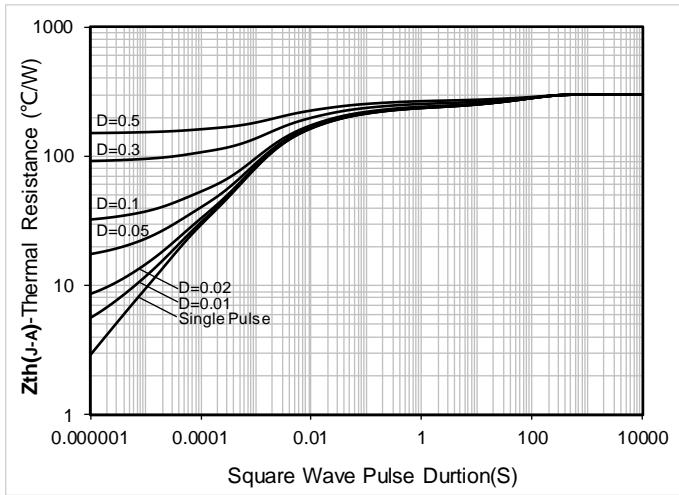


Figure 13. Maximum Transient Thermal Impedance

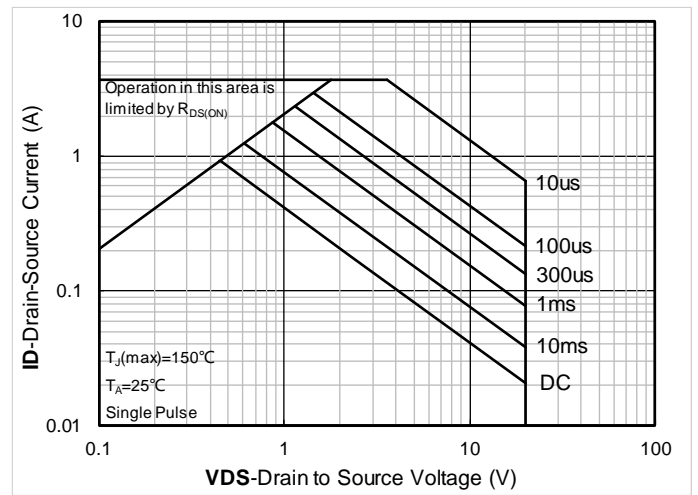
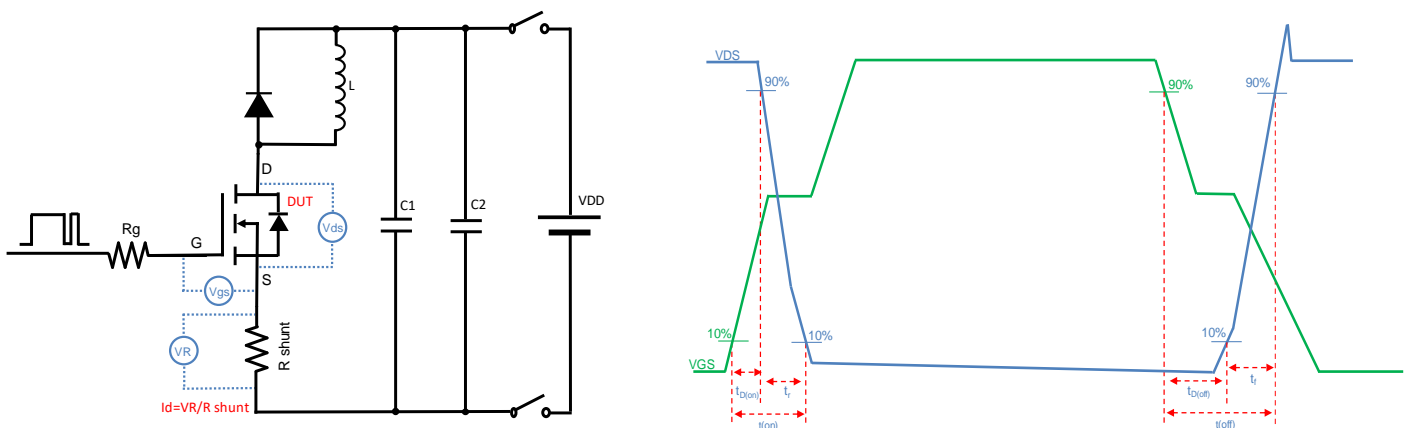
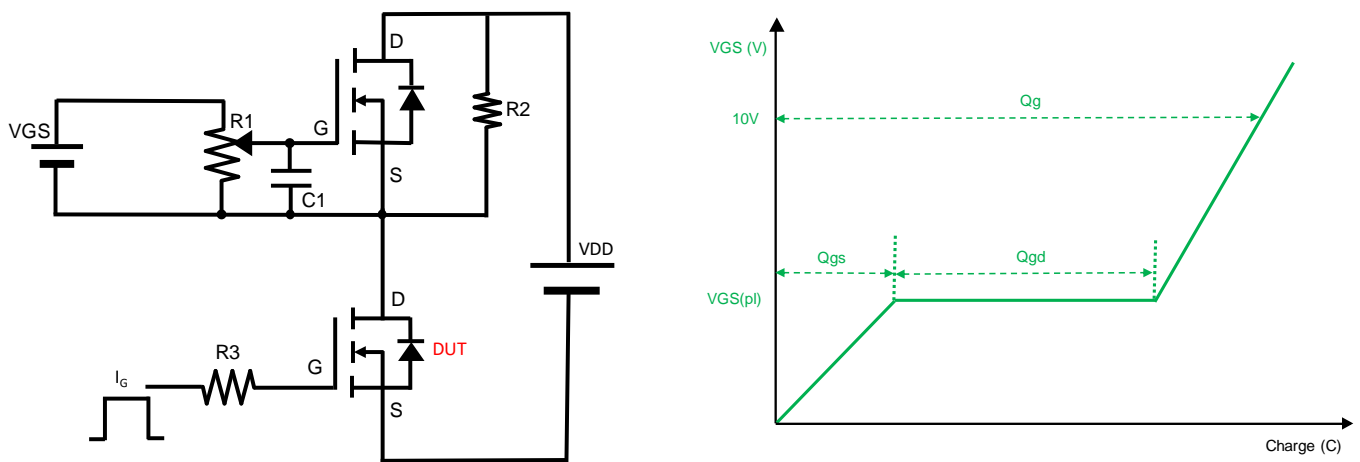
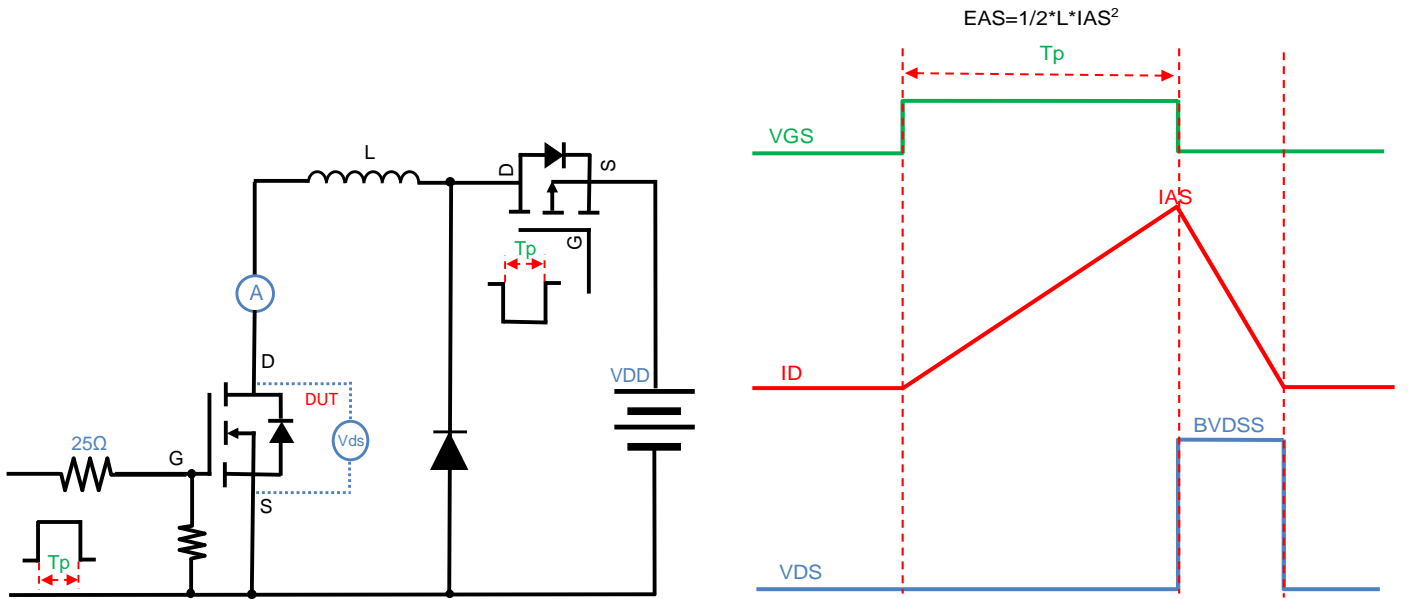


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms



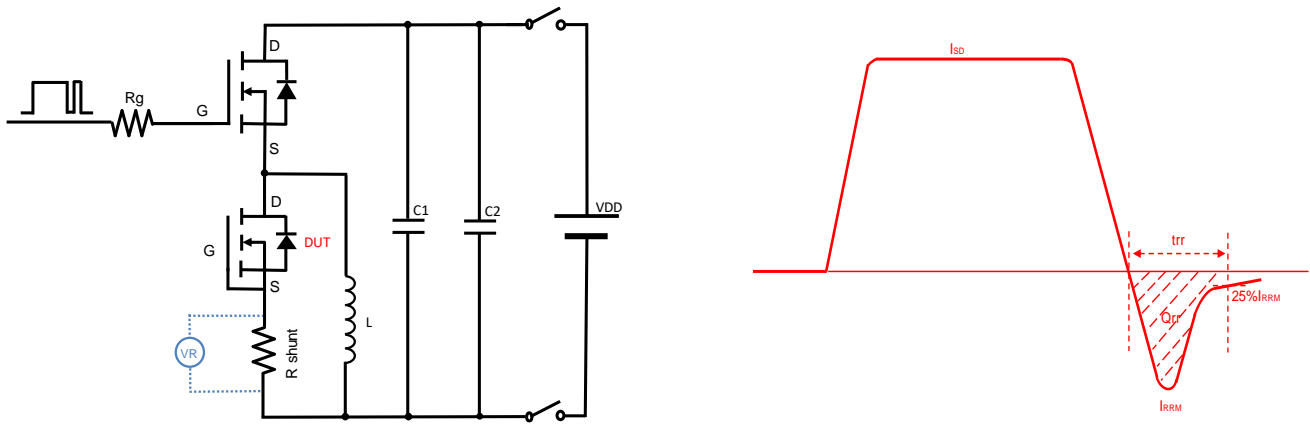
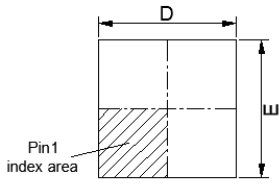


Figure D. Diode Recovery Test Circuit & Waveform

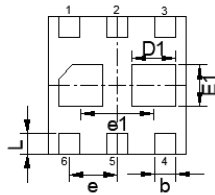


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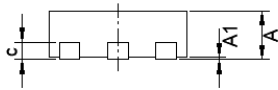
DFN1010B-6L Package information



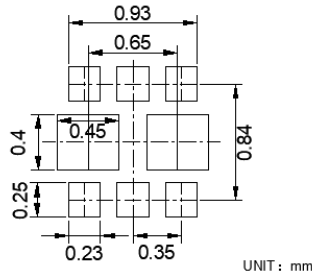
TOP VIEW



BOTTOM VIEW



SIDE VIEW



SUGGESTED SOLDER PAD LAYOUT

UNIT: mm

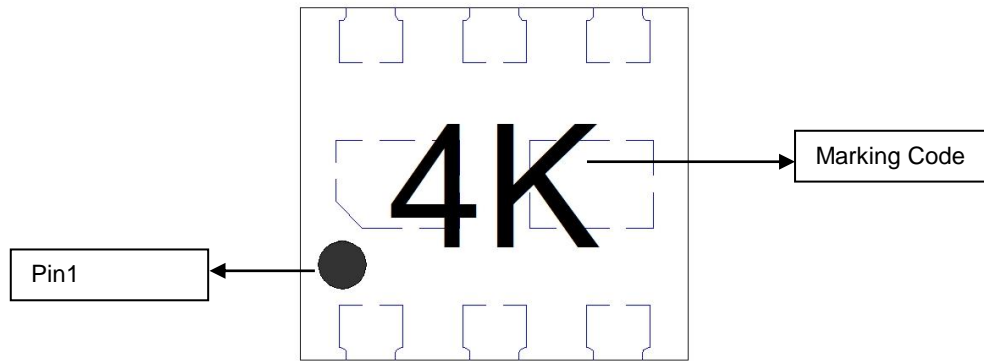
DIM	INCH		MM		NOTE
	MIN	MAX	MIN	MAX	
A	0.011	0.017	0.28	0.43	
A1	0.000	0.003	0.00	0.08	
b	0.003	0.009	0.07	0.23	x6
c	0.005		0.127		TYP
D	0.036	0.043	0.92	1.08	
D1	0.009	0.016	0.24	0.40	x2
E	0.036	0.043	0.92	1.08	
E1	0.009	0.015	0.22	0.38	x2
e	0.014		0.35		TYP
e1	0.021		0.53		TYP
L	0.007	-	0.17	-	x6

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



■ Marking Information



Note:

1. All marking is at middle of the product body
2. All marking is in laser printing
3. 4K is marking code
4. Body color: Black



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